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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,571	BOLCATO ET AL.	
	Examiner	Art Unit	
	CUONG V. LUU	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-7,9-21 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-7, 9-21, and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Comment [H1]: Are the claims statutory? If so, need explanation in action of why. See K's email about 101

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/23/2009 has been entered.

DETAILED ACTION

Claims 1, 4-7, 9-21, and 24-30 are pending. Claims 2-3, 8, and 22-23 have been canceled. Claims 1, 4-7, 9-21, and 24-30 have been examined. Claims 1, 4-7, 9-21, and 24-30 have been rejected.

Process claims 1, 4-7, and 9-10 were also analyzed under 35 USC 101. It is recognized that, in order to be statutory, a process claim must be 1) tied to a particular machine or apparatus, or 2) it transforms a particular article into a different state or thing. *In re Bilski*, 88 USPQ2d 1385 (2008). It is also recognized that a general purpose computer may be converted into a particular computer through the operation of software on the computer. *In re Alappat*, 31 USPQ2d 1545 (1994). For the instant invention, the specification makes clear that the simulation method is carried out via software operating on a computer as described in the specification on page 4 lines 10-26 and page 8 lines 19-24. As such, the process is tied to a particular machine, thus meeting the *Bilski* test.

Response to Arguments

1. Applicant's arguments with respect to claims 1, 4-7, 9-21, and 24-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11-12, 16-17, 20-21, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Pileggi et al. (U.S. Pub. 2003/0046045 A1).

1. As per claim 11, Pileggi teaches a simulator apparatus for simulating a circuit, comprising:

   A computer including a single simulator kernel, the single simulator kernel including (pp. 6-7 paragraph 0060):

   a) an analog solver simulating a first set of circuit nodes and components using time-domain representations of signals (p. 3 paragraphs 0029-0030); and

   b) an RF solver simulating a second set of circuit nodes and components using time-frequency domain representations of signals (p. 3 paragraphs 0029-0030);

   the simulator kernel solving partitioning the circuit, in a single simulation flow, into at least one analog partition including one or more nodes and components from the first set and at least one RF partition including one or more nodes and components from the second set with a solution of the at least one analog partition affecting a solution of the at least one RF partition and vice versa (p. 3 paragraphs 0029-0030 and p.4 paragraphs 0039-0040).

2. As per claim 12, Pileggi teaches an input to read a net list describing the physical characteristics of the circuit (p. 2 paragraph 0026).

3. As per claim 16, Pileggi teaches an input to read an analog database and an RF database (p. 3 paragraph 0030. The teaching of simulating 2 sets of circuit one analog and one RF indicate reading of an analog database and an RF database).

4. As per claim 17, these limitations have already been discussed in claim 11. They are, therefore, rejected for the same reasons.

5. As per claim 20, the discussions in claim 11 inherit the analog solving means and RF solving means within a single simulator kernel.

6. As per claim 21, the discussions in claim 11 imply these limitations. They are, therefore, rejected for the same reasons.

7. As per claim 27, Pileggi teaches:

partitioning the circuit into separate modules coupled together, with each module being associated with at least one boundary node external to the module (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030 and Figure 2);

positioning a boundary node by specifying the boundary node to a fixed value or spectrum (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030 and Figure 2); and

solving a partitioned module using the fixed value or spectrum assigned to the positioned boundary node (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030 and Figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being anticipated by Pileggi in view of the Applicant's admitted prior art, hereinafter AAPA.

8. As per claim 1, Pileggi teaches method of simulating a circuit, comprising:

reading a description of the circuit that includes a list of components in the circuit and the interconnections between the components, the circuit including both a first set of nodes and components responsive to time-domain signals, the time-domain signals comprising analog signals given by V(t), and a second set of nodes and components responsive to time-frequency domain signals (p. 2 paragraph 0026); and

in a single simulation flow, simulating time-domain representations of signals on the first set of nodes and simulating time-frequency domain representations of signals on the second set of nodes by interrelately solving two sets of non-linear equations until convergence, the two sets of equations including a first set of non-linear equations related to the time-domain

signals and a second set of non-linear equations related to the time-frequency domain signals (p. 3 paragraphs 0029-0030 and p.4 paragraphs 0039-0040); and

in the single simulation flow, partitioning the circuit into at least one analog partition including one or more nodes and components from the first set and at least one RF partition including one or more nodes and components from the second set with a solution of the at least one analog partition affecting a solution of the at least one RF partition and vice versa (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030);

but does not teach the time-frequency domain signals comprising RF signals given by $v(t) = \sum V_k(t)e^{j\omega k^{(t)}t}$.

However, the Applicant's admitted prior art teaches this feature (paragraph 0005).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi and the AAPA. The AAPA's teachings would efficiently have handled the modulation information carried by RF signals.

9. As per claim 7, Pileggi teaches:

partitioning the circuit into separate modules coupled together, with each module being associated with at least one boundary node external to the module (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030 and Figure 2);

positioning a boundary node by specifying the boundary node to a fixed value (p. 2 paragraph 0027 and p. 3 paragraphs 0029-0030 and Figure 2); and

solving a partitioned module using the fixed value assigned to the positioned boundary node (p. 3 paragraphs 0029-0030 and Figure 2).

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi in view of the AAPA as applied to claims 1 above, and further in view of Li et al. (A Frequency Relaxation Approach for Analog/RF System-Level Simulation, ACM 2004, 1-58113-828-8/04/0006) and McGauhy et al. (U.S. Pat. 7,143,021 B1).

10. As per claim 4, Pileggi teaches automatically refining the partitions but does not teach the refining is to provide a higher probability of convergence and receiving user input controlling how to partition the circuit.

Li teaches the refining is to provide a higher probability of convergence (col. 1 of p. 843 the 2nd paragraph, p. 846 col. 2 section 4.1 paragraph 2 in this section and Table I. In these paragraphs and Table, Li teaches iteratively partitioning the circuit using relaxation method using a computer. This teaching reads onto the feature),

and McGauhy teaches receiving user input controlling how to partition the circuit (col. 15 lines 46-53. In theses lines McGauhy teaches partitioning of circuit to the preference of end-users. This teaching reads onto this limitation)

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, the AAPA, McGauhy, and Li. McGauhy's and Li's teachings would have facilitated the efficient and accurate analysis of complex response signals over wide frequency ranges (Li, col. 1 of p. 843 the 2nd paragraph) and allowed for users' flexible choosing of what degree of flattening of the circuit partitioning (col. 15 lines 46-53).

11. As per claim 5, the discussions in claim 4 suggest partitioning the circuit based on user input and automatically sub-partitioning the circuit to increase simulation speed.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi in view of the AAPA as applied to claims 1 above, and further in view of Li et al.

12. As per claim 6, Pileggi and the AAPA do not teach simulating comprises solving each of the partitions separately and performing relaxations over all of the solved partitions, but Li teaches this limitation (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, the AAPA, and Li. Li's teachings would quickly have produced a good approximate solution the entire system after several iterations (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi in view of the AAPA as applied to claim 1 above, and further in view of Gabele et al., hereinafter Gabele, (U.S. Pub. 2003/0135354 A1).

13. As per claim 9, Pileggi and the AAPA do not teach receiving, on a server computer, the description from a client computer over a distributed network, simulating the description on the server computer, and returning results to the client computer over the distributed network.

However, Gabele teaches this limitation (paragraph 0349. In this paragraph Gabele teaches a computer, considered a server, receiving description from another computer, considered a client, to run simulation and then returning the results to the former computer).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, the AAPA, and Gabele. Gabele's teachings would have performed simulations of complex and large circuit (paragraph 0008).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi in view of the AAPA as applied to claim 1 above, and further in view of Du (U.S. Pub. 2003/0125914 A1).

14. As per claim 10, Pileggi teaches simulating comprises solving analog and RF partitions for each time step H, but does not teach the time step H is automatically adjusted based on the simulation results of previous time steps and input stimuli ().

Du teaches this limitation (p. 3 paragraphs 0031-0037).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, the AAPA, and Du. Du's teachings would have provided for mixed-signal system simulation that is faster and more adaptable across platforms (p. 4 paragraph 0045).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi as applied to claim 11 above, and further in view of McGauhy et al.

15. As per claim 13, Pileggi does not teach an input to receive control statements from a user to partition the circuit. However, McGauhy teaches receiving user input controlling how to partition the circuit (col. 15 lines 46-53. In theses lines McGauhy teaches partitioning of circuit to the preference of end-users. This teaching reads onto this limitation)

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi and McGauhy. McGauhy's teachings would have allowed for users' flexible choosing of what degree of flattening of the circuit partitioning (col. 15 lines 46-53).

Claims 14, 19, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi as applied to claims 11, 17, and 21 above, and further in view of Li et al. and McGauhy et al.

16. As per claim 14, Pileggi does not teach a partitioner to partition the first and second set of nodes and components into modules in combination with based on user input and to automatically sub-partition the modules to encourage convergence.

Li teaches the refining is to provide a higher probability of convergence (col. 1 of p. 843 the 2nd paragraph, p. 846 col. 2 section 4.1 paragraph 2 in this section and Table I. In these paragraphs and Table, Li teaches iteratively partitioning the circuit using relaxation method using a computer. This teaching reads onto the feature),

and McGauhy teaches receiving user input controlling how to partition the circuit (col. 15 lines 46-53. In theses lines McGauhy teaches partitioning of circuit to the preference of end-users. This teaching reads onto this limitation)

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, McGauhy, and Li. McGauhy's and Li's teachings would have facilitated the efficient and accurate analysis of complex response signals over wide frequency ranges (Li, col. 1 of p. 843 the 2nd paragraph) and allowed for users' flexible choosing of what degree of flattening of the circuit partitioning (col. 15 lines 46-53)

17. As per claim 19, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

18. As per claim 24, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

19. As per claim 25, the discussions in claim 14 suggest partitioning the circuit based on user input and automatically sub-partitioning the circuit to increase simulation speed.

Claims 15 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi in view of as applied to claims 11 and 21 above, and further in view of Li et al.

20. As per claim 15, Pileggi does not teach a relaxation tester coupled to the analog and RF solvers to perform one-step relaxation on results provided by the solvers. but Li teaches this limitation (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

    It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi and Li. Li's teachings would quickly have produced a good approximate solution the entire system after several iterations (col. 1 of p. 843 2nd paragraph of section 2 Latency in Analog/RF Systems).

21. As per claim 26, these limitations have already been discussed in claim 15. They are, therefore, rejected for the same reasons.

Claims 18 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi as applied to claims 17 and 21 above, and further in view of Gabele.

22. As per claim 18, Pileggi does not teach a network and wherein the list is read from a client computer coupled to the network and the means for simulating includes a server computer coupled to the network. However, Gabele teaches this limitation (paragraph 0349. In this paragraph Gabele teaches a computer, considered a server, receiving description from another computer, considered a client, to run simulation and then returning the results to the former computer).

    It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi and Gabele. Gabele's teachings would have performed simulations of complex and large circuit (paragraph 0008).

23. As per claim 29, these limitations have already been discussed in claim 18. They are, therefore, rejected for the same reasons.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi as applied to claim 21 above, and further in view of the AAPA.

24. As per claim 28, Pileggi teaches the time-domain representation of a signal is given by V(t) (p. 2 paragraph 0026) but does not teach the time-frequency domain representation of a signal is given by

$$v(t) = \sum V_k(t)e^{j\omega k^{(t)t}}$$

    However, the Applicant's admitted prior art teaches this feature (paragraph 0005).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi and the AAPA. The AAPA's teachings would efficiently have handled the modulation information carried by RF signals.

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi as applied to claim 21 above, and further in view of Du.

25. As per claim 30, Pileggi teaches simulating comprises solving analog and RF partitions for each time step H, but does not teach the time step H is automatically adjusted based on the simulation results of previous time steps and input stimuli ().

Du teaches this limitation (p. 3 paragraphs 0031-0037).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Pileggi, the AAPA, and Du. Du's teachings would have provided for mixed-signal system simulation that is faster and more adaptable across platforms (p. 4 paragraph 0045)...

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Cuong V Luu/

Examiner, Art Unit 2128

/Hugh Jones/

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